Computer Architecture and Logic Design

Code	Credit Hours
EE- 122	3-1

Course Description

This course focuses on the principles, current practices, and issues in Logic Design and Computer Architecture. To build the foundation of the course, Logic Design will be introduced with the logic operators and gates to lay the framework for strengthening the basic understanding of computer building blocks. Both combinational and sequential circuits are studied in this course along with their constituent elements comprising Arithmetic circuits, Comparators, Decoders, Encoders, Multiplexers, Tri-state gates as well as Latches, Flip-flops, Counters and Registers. In this course students will learn the principles of Computer Architecture and Logic Design. They will combine classical design methodologies with a series of laboratory assignments in which they will demonstrate their ability to successfully design, implement, and debug digital systems using Computer Aided Design tools and physical prototyping.

Text Book:

1. M. Morris Mano and Michael Ciletti, Digital Design, 5th Edition
2. Hennessy and Patterson, Computer Organization and Design: The Hardware/Software Interface, RISC-V Edition (2nd)
3. Sarah and Harris, Digital Design and Computer Architecture, RISC-V Edition (1st)

Reference Book:

1. Yale N. Patt and Sanjay J. Patel, Introduction to Computing Systems, 2nd Edition
2. Hennessy, Patterson, Computer Architecture: A Quantitative approach, 6th Edition

Prerequisites

None

ASSESSMENT SYSTEM FOR THEORY

Quizzes	10%
Assignments	10%
Mid Terms	30%
ESE	50%

ASSESSMENT SYSTEM FOR LAB

Quizzes	10%-15%

Assignments	5% - 10%
Lab Work and Report	70-80%
Lab ESE/Viva	20-30%

Teaching Plan

Week No	Topics	Learning Outcomes
1	Introduction	Course Outline, objectives, teaching plan, assessment method, motivation to course
2-6	Binary Number System, Boolean Logic Combinational Logic Circuit Design	Introduction to binary numbers and different binary representations Introduction to Boolean logic and Boolean Algebra Learning to design basic logic gates and simplify logic Learning the basic principles in combinational circuit design K-maps, Sum of product and product of sum form to derive combinational logic circuit expressions
7-8	Sequential Logic Circuit Design	Learning about memory elements, basic latches and flip-flops Learning about sequential circuits, Moore's and Mealey's machine Learning about Finite State Machine Design Learning about FSM Timing
9	**MID TERM EXAM**	
10-12	Introduction to Processor Design and Computer Architecture	Building a simple processor bottom-up Learning about machine language, assembly language and compilation
13-17	Practical Processor Design	Learning about a practical ISA and assembly language Instruction types, addressing modes and machine encodings Implementation of a single-cycle processor

		Implementation of a pipelined processor Dealing with pipeline hazards
18	**End Semester Exams**	

Practical:

Experiment No	Description
1	Familiarization of Basic Gates and Digital ICs, Introduction to Verilog HDL. Basic language constructs and design entry using Verilog HDL.
2	Derivation of Boolean Functions from given logic diagram and its Hardware implementation. Verilog HDL Gate-Level modeling.
3	Verilog Coding Using Dataflow Modeling Technique
4	Design of Simple Practical Circuits
5	Binary to Gray and Gray to Binary Code Conversion
6	2-bit binary Adder and Subtractor
7	Design of Voting Machine
8	Design of Sequence Detector
9	Implementing an ALU
10	Design of Mini-Processor
11	Design of single cycle processor
12	Lab Exam